IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF: :

Warren SNYDER et al.   : GROUP ART UNIT: #3/

SERIAL NO: 09/975,030   :

FILED: OCTOBER 10, 2001   : EXAMINER:

FOR: EMULATOR CHIP/BOARD
       ARCHITECTURE AND
       INTERFACE

PRELIMINARY AMENDMENT

COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

Prior to examination of the above-identified application, consideration of the following

Amendments and Remarks is respectfully requested.

IN THE SPECIFICATION

Please replace the paragraph at page 1, lines 11-28 with the following paragraph:

This application is related to U.S. Patent Application Serial No. 09/975,115, docket

number CYPR-CD00182, to Warren Snyder, et al., entitled "IN-SYSTEM CHIP EMULATOR

ARCHITECTURE"; and to U.S. Patent Application Serial No. 09/975,104, docket number

CYPR-CD00183, to Warren Snyder, entitled "CAPTURING TEST/EMULATION AND

ENABLING REAL-TIME DEBUGGING USING AN FPGA FOR IN-CIRCUIT

EMULATION"; and to U.S. Patent Application Serial No. 09/975,338, docket number CYPR-

CD00186, to Warren Snyder, et al., entitled "METHOD FOR BREAKING EXECUTION OF

(TEST) CODE IN A DUT AND EMULATOR CHIP ESSENTIALLY SIMULTANEOUSLY